6. (Original) The apparatus of claim 5, wherein the combining circuit comprises a summation element for forming a sum of transition values and decision logic for comparing the sum to a threshold value.

7. (Original) The apparatus of claim 6, wherein the threshold value is set in accordance with an anticipated frequency range of the unknown clock signal.

8. (Currently Amended) A method of forming a number stream representing frequency or phase of digital or digitized clock signals using a digital circuit, one of the clock signals being a known clock signal and another of the clock signals being an unknown clock signal, comprising:

applying to the digital circuit an alias value indicating an expected frequency range of ~~the~~ a received unknown clock signal; and

forming the number stream in accordance with the alias value, said number stream representing the frequency or phase of the unknown clock signal.

9. (Currently Amended) A digital circuit for forming a number stream ~~for~~ representing frequency or phase of ~~digital or digitized clock signals, one of the clock signals being a known clock signal and another of the clock signal being~~ an unknown clock signal, comprising:

a first logic section including multiple chains of flip flops, each chain producing an intermediate value[[s]] for each period of a known clock signal; and

a second logic section ~~for~~ configured to receiv~~inge~~ an alias value indicating an expected frequency range of ~~the~~ ~~an~~ the unknown clock signal and, in successive cycles of the known clock signal, ~~and~~ operable to compare the alias value to sums of the intermediate values produced by said multiple chain of flip-flops ~~combining the intermediate values~~ to form the number stream.